Development of QPSK Demodulator using DSP Techniques

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Abstract

This paper presents the design and implementation of the QPSK demodulator using digital signal processing techniques. The QPSK demodulator is designed and implemented using two different approaches. In the first approach, digital filters are used for implementing the demodulator. In the second approach, the DFT is used for implementing the demodulator. The first approach is performed using digital low-pass filters, Costas loop, and NCO. In the second approach, the DFT is used in development of the QPSK demodulator by computing the spectrum of the coming modulated signal and finding the maximum peak of the spectrum as it is used to determine the carrier frequency and its phase. The data bits are then determined from the phase of the carrier. Both approaches are implemented using python software and raspberry pi processor for to be used as embedded system and also as experimentation. Both design methods are tested and verified through simulation experiments.

Keywords

QPSK demodulator, DSP application, Phase-Shift Keying, DFT method, Costas loop , and digital filter.

1- Introduction

The idea of modulation is a key factor in communication systems, on the grounds that without a fitting modulation technique or plan, getting a normal throughput in such a communication exertion would be difficult to accomplish. Communication designers and specialists have not yielded in endeavoring to locate the best modulation strategies went for accomplishing a normal throughput, transmission capacity/control proficiency, low error execution, and so on in digital communication systems. Digital modulation is like the analogue modulation because of their blunder free capability. More so, this decision of digital modulation is subject to the kind of communication network that will be set up. Be that as it may, exchange offs must be made between the transmission capacity productivity,

control proficiency and the cost of usage of such a system. Therefore, this study begins with the presentation of digital modulation types, and then the adjustment of the quadrature phase shift keying (QPSK). The next generation of wireless communication systems requires higher data transmission rates in order to meet the higher demand of quality services [1]. Communicating effectively over a huge distance has always been the challenge for engineers and scientists and with the transition of modulation systems from analog to digital has further complicated the situations. The transition from analog to digital modulation provides more information capacity, Compatibility with digital data services, advanced data security, faster system availability and better- quality communications [2].

In the last few decades, a major transition from analog to digital communications has occurred and it can be observed in all fields of communications because digital communication system is more reliable than an analog system [3]. Digital modulation schemes provide more information carrying capacity, better quality communication, and data.

Because of its relationship to complex-envelope representations of signals, quadrature modulation plays a central role in simulation of wireless communication systems and models for quadrature modulators, and demodulators serve as building blocks for most other types of data modulators and demodulators.

The progress from simple modulation techniques to digital modulation provides more data limit similarity with digital information administrations, higher information security, better quality communication, and faster framework accessibility [4]. Be that as it may, designers of communication frameworks face such limitations as accessible data transfer capacity, and reasonable power.

Digital modulation plans have more prominent ability to pass on a lot of data than simple modulation plans [5], [6]. Digital modulation has intrinsic advantages over analogue modulation since its unmistakable transmission states would more be able to effortlessly be distinguished at a collector within the sight of commotion than analogue signal, which can expect a vast number of qualities. Then again, when a carefully transmitted signal begins as a simple waveform, an exchange off happens since some data is continuously lost in the quantization procedure important to change over the simple flag to a digital one[6],[7]. The different modulation plans offered distinctive arrangements as far as cost-viability and nature of got signal, data transfer capacity productivity and power effectiveness however as of not long ago were still to a great extent simple. Frequency modulation and phase modulation displayed certain invulnerability to commotion though amplitude modulation was less complex to demodulate .Notwithstanding, more as of late with the appearance of low-cost microcontrollers and the presentation of household cell phones and satellite. Interchanges, computerized balance has picked up ubiquity. With digital modulation systems come every one of the preferences that conventional microchip circuits have over their simple partners. Any deficits in the communication connection can be annihilated utilizing programming. Data would now be able to be scrambled, blunder rectification can guarantee more trust in gotten information, and the utilization of digital signal processing (DSP) systems can diminish the restricted

data transfer capacity assigned to each administration [8].

Digital modulation plans are arranged the previously mentioned methods for modulation. The first of the plans is the amplitude modulation which comprises of the OOK [On and Off Keying] which is the most straightforward type of amplitude modulation which is otherwise called 2-ASK i.e. amplitude shift Keying that differs between two states. Higher-arrange ASK modulation conspire is QAM [Quadrature Amplitude Modulation] which has different sub-plans like 8QAM, 16QAM, 32QAM 64QAM and so on. However, amplitude modulation is low as frequency and phase modulation procedures offer greater resistance to noise, they are the favored plans for the greater part of administrations being used today.

Frequency modulation offers FSK [Frequency Shift Keying] that is separated into different plans like: [QFSK, 8-FSK, 16-FSK] and so forth while the third digital modulation procedure phase and it is called 'phase Shift Keying' which offers different plans like: BPSK, DPSK, QPSK, 8-PSK, 16-PSK and so forth.

2-Digital Modulation Methods

In digital modulation, an analog carrier signal is modulated by a digital bit stream of either equal length signals or varying length signals. This can be described as a form of analog-to-digital conversion. The changes in the carrier signal are chosen from a finite number of alternative symbols (the modulation alphabet).there are the most fundamental digital modulation techniques.

In the case of PSK, a finite number of phases are used. In the case of FSK, a finite number of frequencies are used. In the case of ASK, a finite number of amplitudes are used.

2-1 Amplitude-shift keying

The simplest digital modulation technique is amplitude-shift keying (ASK), as shown in figure.1, where a binary information signal directly modulates the amplitude of an analog carrier. ASK is similar to standard amplitude modulation except there are only two output amplitudes "possible" .Amplitude shift keying is sometimes called digital amplitude modulation (DAM) [9].

Fig 1:ASK modulated Signal

FSK is a form of constant-amplitude angle modulation similar to standard frequency modulation (FM) except the modulating signal is a binary signal that varies between two discrete voltage levels rather than a continuously changing analog wave form as shown in figure2[9] .

Fig 2:FSK modulated Signal

Where $s_0(t) = A\cos(\omega_c - \Delta\omega)t$ and $s_1(t) = A\cos(\omega_c + \Delta\omega)t$

2-3Phase Shift keying (PSK)

This is a digital modulation technique that passes on information by changing the period of a reference flag (the carrier wave). PSK utilizes a limited number of phases; each appointed a novel example of twofold bits as shown in figure3.

Normally each stage encodes an equivalent number of bits. Each example of bits shapes the image that is spoken to by the specific stage. The demodulator, which is planned particularly for the image set utilized by the modulator, decides the period of the received signal and maps it back to the image it speaks to, accordingly recouping the first information. This requires the beneficiary to be capable to look at the period of the received signal with a reference signal [10].

Fig 3:PSK modulated signal

where $s_0 = -A\cos(\omega_c t)$ and $s_1 = A\cos(\omega_c t)$

2-3-1Binary Phase-Shift Keying (BPSK)

BPSK is the most straightforward type of PSK. It utilizes two stages which are spoken to by 180 degrees thus can likewise be named 2 – PSK. It doesn't especially make a difference precisely where the heavenly body focuses are situated, and in figure 4 they are appeared on the genuine pivot at 0 degrees and 180 degrees. This modulation is the most hearty of all the PSKs since it takes genuine bending to influence the demodulator to achieve an off base choice. It is, however just ready to balance at 1 bit/image (as found in figure 4) and is so reasonable for high information rate applications [11],[12].

Fig 4: Binary Phase-Shift Keying (BPSK)

2-3-2-Quadrature Phase-Shift Keying (QPSK)

QPSK is a M-ary encoding plan where $N = 2$ and $M = 4$ (henceforth, the name "quaternary" signifying "4"). A QPSK modulator is a double (base 2) signal, to deliver four unique input mixes, : 00, 01, 10, and 11 as found in figure 5. Hence, with QPSK, the twofold information are consolidated into gatherings of two bits, called charges. In the modulator, each charge code produces one of the four conceivable yield phases, ($45^\circ, 135^\circ, -45^\circ$, and -135°). [13]

Fig 5: Quaternary Phase-Shift Keying

In QPSK two progressive bits are joined this mix of two bits shapes four particular symbols. At the point when symbol is change to next symbol the period of the transporter changed by 45° ($\pi/4$ radians).

As shown in figure 6, the QPSK has twofold data transmission effectiveness of BPSK. In mapping of I and Q NRZ organize is fundamental. The QPSK signal is spoken to numerically in underneath condition (1) and I/Q are characterized in condition (2).

$$\text{QPSK}(t) = I(t) \cos(2\pi f_c t) + Q(t) \sin(2\pi f_c t) \quad (1)$$

$$I = \sqrt{2E/T} \cos[(2i-1)\pi/4] \quad (2)$$

$$Q = \sqrt{2E/T} \sin[(2i-1)\pi/4] \quad (3)$$

Fig6:QPSK Modulator

3-QPSK transmitter

The input is a stream of binary digits, this stream is converted into two separate bit streams of $R/2$ bps each, by taking alternate bits for the two streams. The two data streams are referred to as the I (in-phase) and Q (quadrature phase) streams. As shown in figure 7, the upper stream is modulated on a carrier of frequency f_c by multiplying the bit stream by the carrier. This same carrier wave is shifted by 90° and used for modulation of the lower binary stream. A binary 1 is represented by a scaled version of the carrier wave and a binary 0 is represented by a scaled version of the negative of the carrier wave, both at a constant amplitude [15]. Fig. 8 presents Simulated-QPSK-waveforms-at-the-transmitter-side.

Fig 7:Block diagram of QPSK transmitter

Fig.8:Simulated-QPSK-waveforms-at-the-transmitter-side.

4- QPSK receiver

The piece graph of a QPSK receiver is appeared in block diagram of QPSK receiver as shown in Fig.9. The power splitter guides the information QPSK signal to the I also, Q signal and the carrier recovery circuit. The carrier recovery circuit imitates the first transmit transporter oscillator signal. The recuperated transporter must be recurrence and phase reasonable with the transmit reference carrier. The QPSK signal is demodulated in I and Q item indicators, which create the first I and Q information bits. The yields of the item indicators are bolstered to the bit Consolidating circuit, where they are changed over from parallel I and Q information channels to a single parallel yield information stream.[18]

Fig 9:Block diagram of QPSK receiver

5-The QPSK Demodulator

The carrier has to be recovered from the QPSK signal. Then the QPSK signal is multiplied with two carriers. By multiplying the cosine carrier with QPSK modulated data, we can get the raw I-data. Similarly, by multiplying the sine carrier with QPSK modulated data, we can get the raw Q-data. These raw data are then passed through low pass filter and through a comparator to get well shaped data, as shown in Fig.10. Then the I-data and Q-data can be found. The parallel I-data and Q-data are then converted to serial data to achieve the actual signal.

Fig10: Block diagram of a QPSK Demodulator

5-1Mixer for QPSK demodulator

In a coherent detection system, multiplier has great significance. It is the prerequisite to obtain raw data from the modulated signal. A lot of ICs may be used for the purpose of multiplication.

Fig.11. shows the use of the mixer in the modulation circuits.

Fig 11:Block diagram of mixer

5-2Low pass filter (LPF)

Digital FIR low pass filters are used to remove the double frequency components.

The purpose of loop filter is to filter the phase error signal in order to provide a better signal to the VCO. The error signal generated by the phase detector(PD) is

actually a noisy estimate of the phase error, the error signal consists of an error term and a noise term. The loop filter processes the error signal in order to generate a useful error while suppressing the effect of the noise as much as possible.

The loop filter is essentially a low pass filter and a simple filter integrating 16 samples is used as loop filter. A 16-tap FIR filter with all coefficients set to '1' is used as loop filter. Hence the gain of the loop filter is 16.

5-3 Voltage controlled oscillator (VCO)

Voltage controlled oscillator is a type of oscillator where the frequency of the output oscillations can be varied by varying the amplitude of an input voltage signal. Voltage controlled oscillators are commonly used in frequency (FM), pulse (PM) modulators and phase locked loops (PLL). Another application of the voltage controlled oscillator is the variable frequency signal generator itself.

5-4 Costas loop

Costas loop is a kind of closed loop auto tracking system that can be applied in tracking the input signal's phase. The Costas loop performs both phase coherent suppressed carrier reconstruction and synchronous data detection within the loop. It is widely used in fields of radio technology and has become an indispensable part of communication radar, navigation, electronic equipment and other devices. It performs a quadrature mix between a reference oscillator waveform and a received waveform to form two error signals, which when multiplied together creates a suitable signal for adjusting the Voltage Controlled Oscillator (VCO)[16].

Fig 12: Block diagram of Costas loop

Fig.12 shows the basic block diagram of Costas loop, the input signals are sent to two multipliers. The upper called in-phase branch and the lower called quadrature branch. The in-phase branch multiplies input by VCOs output, the quadrature branch multiplies the input by VCOs output after 90° phase shift. The multiplier outputs of the in phase and quadrature branches are passed through the low-pass filter, then multiplied together to get the error signal. The error signal is filtered by the loop filter, whose output is the control voltage which controls VCOs phase and frequency. The following equations show how Costas loop operates.

The input signal to Costas loop is:

$$y(t) = s(t)\cos(\omega_c t + \theta) \quad (4)$$

And let the VCO outputs be,

$$v_1(t) = k \cos(w_c t + \theta_1) \quad (5)$$

$$v_2(t) = k \sin(w_c t + \theta_2) \quad (6)$$

The phase difference between the local carrier and the input carrier is

$$\Delta\theta = \theta - \theta_1 = \theta - \theta_2$$

The output signal after the multiplication is,

$$\begin{aligned} X_I(t) &= s(t)\cos(w_c t + \theta) * k \cos(w_c t + \theta_1) \\ &= \frac{1}{2} k s(t) [\cos\Delta\theta + \cos(2w_c t + \theta + \theta_1)] \end{aligned} \quad (7)$$

$$\begin{aligned} X_Q(t) &= s(t)\cos(w_c t + \theta) * k \sin(w_c t + \theta_2) \\ &= \frac{1}{2} k s(t) [\sin\Delta\theta + \sin(2w_c t + \theta + \theta_2)] \end{aligned} \quad (8)$$

The LPF output is given by,

$$I(t) = \frac{1}{2} k s(t) \cos\Delta\theta \quad (9)$$

$$Q(t) = \frac{1}{2} k s(t) \sin\Delta\theta \quad (10)$$

The phase error signal (Δ) is given by,

$$V_F(t) = \frac{1}{8} k^2 s^2(t) \sin 2\Delta\theta \quad (11)$$

v_f controls the VCO through the Loop

Filter. After several cycles, $\Delta\theta$ changes very small, $\sin \Delta\theta = \Delta\theta$, the phase error gradually is reduced to very small values finally. This time, $v_1(t)$ is the synchronization carrier we need; $I(t)$ is the demodulator output signal. If there is a phase difference, a non-zero control voltage will be generated and the frequency of the oscillator will be adjusted accordingly. In the lock state the control voltage vanishes and the frequency of the oscillator remains unchanged. The quadrature branch of the Costas loop thus tracks the frequency and phase of the carrier while the in-phase of the Costas loop yields the baseband signal [17].

6-Discrete Fourier Transform (DFT)

The discrete Fourier transform (DFT) converts a finite sequence of equally spaced samples of a function into the list of coefficients of a finite combination of complex sinusoids, ordered by their frequencies, that has those same sample values. It can be said to convert the sampled function from its original domain (often time or position along a line) to the frequency domain.

The DFT is the most important discrete transform, used to perform Fourier analysis in many applications[24]. In digital signal processing, the function is any quantity or signal that varies over time, such as the pressure of a sound wave, a radio signal, or daily temperature readings, sampled over a finite time interval (often defined by a window function). In image processing, the samples can be the values of pixels along a row or column of a raster image. The DFT is also used to efficiently solve partial differential equations, and to perform other operations such as convolutions or multiplying large integers.

The DFT is used in developing the QPSK demodulator by computing the spectrum of the coming modulated signal and find the maximum peak of the spectrum where it is used to determine the carrier frequency and its phase. The data bits are then determined from the phase of the carrier.[25]

7-Theproposed design and implementation of the QPSK demodulator

In this research work, the QPSK demodulator is designed and implemented using two methods. The first method is with digital filters and the second method is with

Discrete Fourier Transform (DFT). These two methods are explained in the following two subsections.

7-1 Design and implementation using digital filters

In this method, FIR low pass filters of order 16 are used for implementing the QPSK demodulator as shown in Fig.13. The numerical controlled oscillator (NCO) is a digital circuit that creates two cosine waves of the same frequency with two potentially independent phases. You can use the Carrier Frequency property attribute to set the carrier frequency. The I phase cosine waveform is multiplied by the I signal path, and the Q phase cosine waveform is multiplied by the Q data path. The I and Q phases are programmable from -180° to 180° by setting the Carrier Phase I and Carrier Phase Q properties. Both the frequency and the phases can be updated during generation. For QPSK set the I phase to 0° and Q phase to -90° . The Carrier Phase I/Q properties can be used to simulate quadrature impairments. Change the I or Q Carrier Phase by the required quadrature skew to simulate this impairment.

Architecture of NCO is being adapted in the design of the Costas loop. The architecture of a counter-based NCO is being discussed and the architecture is depicted in fig.14. The input control word is 2-bits wide derived from the first two bits of the 16-bits wide output from the loop filter. The NCO is designed to produce the desired output frequency.

Fig13:Block diagram of digital QPSK Demodulator

Fig .14Block diagram of NCO

7-2 Design and implementation using the DFT method

In this method the FFT of length 1000 points is used to compute the spectrum of the received modulated signal. The carrier frequency is determined from the spectrum of the received signal and then the phase of the carrier is used to recover the I and Q data. The I and Q data are then combined to form the final received data.

The procedure for implementing the quadrature phase shift keying (QPSK) demodulator is shown through the design of the QPSK demodulator and using the Python program.

A discrete Fourier transform unit for receiving the phase modulation signal to be demodulated, and means of recovering the carrier frequency of the phase modulation signal, so that the discrete Fourier transform unit performs in combination the operations of mixing and low-pass filtering the sampled phase modulation signal with at least one frequency and phase adapted digital conversion signal to supply at least one demodulated signal at the output of the discrete Fourier transform unit.

One advantage of the DFT lies in the fact that instead of the conventional at least one mixer and at least one low-pass filter, there is provided a discrete Fourier transform unit, which combines the mixing and low pass filtering operations. With the discrete Fourier transform unit ,it is therefore possible to perform digital demodulation of the phase modulation signal to provide at least one demodulated signal, wherein the carrier frequency of the phase modulation signal has been removed.

8-Simulation Results

The two design methods, the filter based method and the DFT method, are implemented using Python software. The two implementation methods are tested and they gave the same results as shown in Fig.15. This figure shows the binary data to be transmitted, the non-return to zero signals, the transmitted signal, the received signal and the recovered data. As it can be seen from the figure, the recovered data is identical to the transmitted data.

The qpsk demodulator is modeled using python for carrier frequency 10 MHz ,The simulation results (Fig. 15) shows that the modulated data is the same as the modulating data.

Fig. 15: QPSK Transceiver

10-Conclusion

The design and implementation of qpsk demodulator is developed. The qpsk demodulator is design and implemented using digital filter technique and DFT technique. The QPSK demodulator was developed and tested using python software and implemented using raspberry pi processor. In the DFT technique, the carrier phase was detected from the output of the DFT. The data transmitted is detected from the phase information of the carrier obtained from the DFT.

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